

INTRODUCTION

The WL102 Development Board has been developed to provide a flexible development platform for the WL102 Wireless Data Controller.

Available in the form of full schematic and PCB layout design data, the WL102 Development Board allows developers to evaluate the WL102 and to develop a wireless data system utilising any of the device's configuration options.

The Development Board is 24cm by 13cm in size, and features a socketed 144-pin WL102. Fig. 1 shows a block diagram of the system.

Also provided is supporting software to allow in system programming of the Flash ROM via the Host interface.

SYSTEM PROCESSOR

As well as the WL102's internal 8051 processor, the developer may instead use an external 8051 compatible device (or in circuit emulator) via the 40 pin DIL socket.

Also provided is a 64way (DIN 41612) edge connector for interfacing other external processor systems. This interface also provides:

- A 10MHz clock output
- Active high and active low reset outputs
- Access to the full 128KBytes of the Flash ROM
- Dedicated Address/Data buses or a multiplexed Low Address and Data bus. (with on board latch)

For added flexibility on board level translation logic allow the external processor to operate at a supply voltage of 5 volts although that of the WL102 and radio transceiver may be 3 volts.

PROGRAM ROM

The board features a 128 Kbyte Flash ROM for program storage. DIL and TSOP footprints are provided.

HOST INTERFACE

Two 34 way (IDC) connectors provide access to the HOST interface of the WL102.

These connectors are configured so as to allow the board to be used in a PC Card socket (via a suitable adapter).

RADIO INTERFACE

The WL102 Development Board supports both the DE6003 and the WL600/WL800 RF Development Board. On board buffering is provided for the DE6003 Clock and Received Data signals.

POWER SUPPLY REGULATION

The WL102 Development Board is fitted with two voltage regulators, providing 5 volt and 3 volt power supplies which may be used to provide the Host interface, System, Radio and external processor supplies.

The board may also be powered directly from the Host Interface.

OPTIONAL COMPONENTS

System Clock

The WL102 system clock may be generated from either the radio transceiver board or by an on board oscillator module.

External Data RAM

The WL102 Development Board may be fitted with an external 32 Kbyte SRAM which is decoded into an unused portion of the WL102 address map. DIL and TSOP footprints are provided.

External Buffer RAM

The WL102 Development Board may be fitted with an external 32Kbyte SRAM for expansion of the WL102 shared buffer. DIL and TSOP footprints are provided.

Analog To Digital Converter

The WL102 Development Board may be fitted with a Harris CA3306 (or compatible) ADC device which is decoded into the RSSI_STROBE are of the WL102 address map.

WL102

RS-232 Interface

A Maxim MAX3221 RS-232 line driver may be fitted to the board to provide a serial interface to the System processor

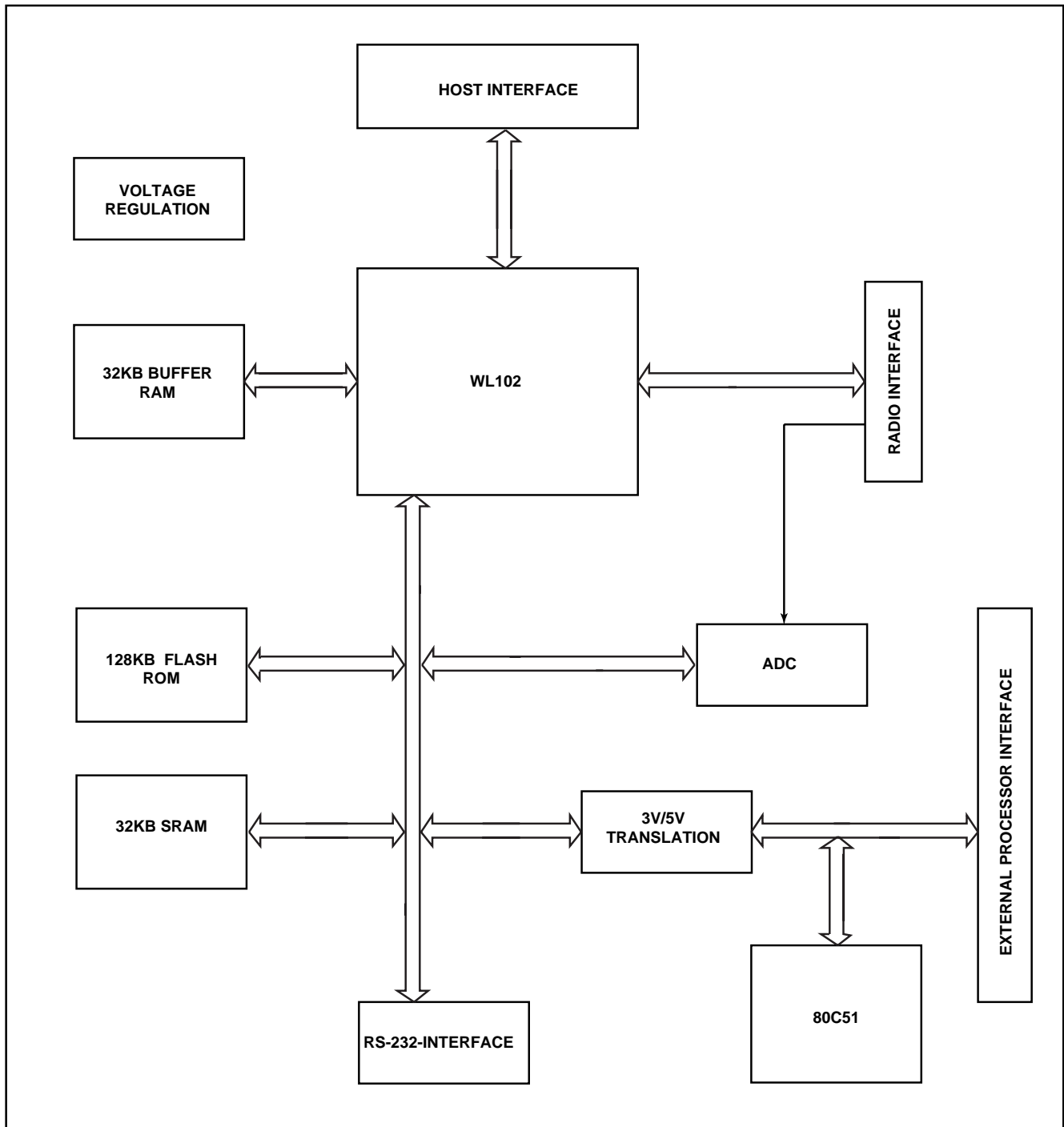


Fig. 1 Development board block diagram



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